

# SPECIFICATION

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## ***LIQUID CRYSTAL DISPLAY DRIVER AND METHOD THEREOF***

### Background of Invention

[0001] *FIELD OF THE INVENTION*

[0002] The present invention relates to a liquid crystal display and pulse generation circuit for displaying images on the basis of input video signals, and more particularly to a liquid crystal display and pulse generation circuit in which the number of switching times for pulse strings is improved.

[0003] *BACKGROUND OF THE INVENTION*

[0004] In general, when an image is displayed on a liquid crystal display (LCD), image signals are output from a graphics controller in a system unit or system part of a PC or the like via a video interface. An LCD controller LSI, which receives these image signals, supplies signals to each IC in a source driver (i.e., X driver, LCD driver) and gate driver (i.e., Y driver), and then a voltage is applied to each source electrode and each gate electrode in a TFT array arranged in a matrix fashion, thereby leading to displaying images.

[0005] As a configuration employed in this LCD source driver, technologies called chip-on-glass (COG) and wiring-on-array (WOA) have recently become the focus of attention. Also, a technology is being developed where a driver LSI is arranged in a TCP (tape carrier package) and connected to the TFT array substrate (glass substrate) via the TCP. It is expected that manufactures' costs will be reduced by applying these technologies to attach ICs directly on the glass substrate or via the TCP as well as to eliminate wiring on a printed circuit board.

[0006] On the other hand, there are mainly two types of digital-analog conversion

circuits (DAC): one is a current summing scheme such as an R-2R ladder network type DAC in which there are provided as many current sources as the number of bits of digital input data, wherein the current is added depending on a value of each bit of the input data in order to obtain an output current corresponding to the input data; the other is a time control scheme such as an integral type DAC in which an output voltage is obtained by charging a capacitor for a time depending on the digital input data with a constant current. Furthermore, the time control scheme includes a pulse width modulation (PWM) type DAC in which an output voltage is obtained by integrating a pulse string whose duty is adjusted depending on the digital input data, and a pulse density modulation (PDM) type DAC in which an output voltage is obtained by integrating a pulse string wherein the number of pulses occurring within a predetermined time is adjusted depending on the digital input data.

[0007] In order to implement a reference voltage generation circuit for gamma correction that is built in the LCD source driver, in order to reduce the deviation of the reference voltage between drivers, these PWM or PDM type DACs are used. These DACs have a high applicability to LCDs since they are of the above-mentioned time control scheme, wherein a difference of the output voltage is unlikely to be introduced due to dispersion of resistors and capacitors created in the chip.

[0008] Fig. 13 depicts a configuration of a typical PDM type DAC. The PDM type DAC comprises a pulse generation circuit 201 for generating a plurality of reference pulses in which pulse generation densities are weighted, a digital input data latch 202 for storing digital input data, a pulse select/synthesis circuit 203 for generating a pulse string by selecting and synthesizing necessary reference pulses on the basis of generated reference pulses and input data, a voltage conversion circuit 204 for converting a pulse string generated by a digital power supply into a desired analog voltage range, and an integration circuit (low pass filter) 205 for converting a pulse string into an analog voltage.

[0009] For a PDM type DAC as shown in Fig. 13, since a frequency of the pulse string is able to be increased compared with a PWM type DAC, resistors and capacitors used in integration circuit 205 are reduced, which preferably makes a chip area small, thereby saving costs. On the contrary, power consumption is increased due to the increase of

frequency of the pulse string, and moreover the linearity of the output voltage is deteriorated because the number of switching times differs for pulse strings corresponding to each of digital input data.

[0010] Fig. 14 depicts a schematic diagram of pulse generation circuit 201 for use in a PDM type DAC for liquid crystal displays. The circuit shown in Fig. 14 is used in the case of 9 bit DAC, which comprises a 9 bit binary counter 210, a 9 bit latch 211, and nine 2-input AND gates 212. By ANDing counter outputs from binary counter 210 with negative latched outputs from 9 bit latch 211, weighted pulses are generated at the reference pulse outputs X8 through X0. Assuming the pulse density of X0 is 1, those of X1, X2, X3, X4, X5, X6, X7 and X8 are 2, 4, 8, 16, 32, 64, 128, 256, respectively. It is also noted that since the reference pulses X0 through X8 are generated such that they become high exclusively, these pulses never overlap temporally each other even if any plural number of reference pulses are synthesized.

[0011] Fig. 15 depicts a waveform of pulse outputs (X8 through X0) of a PDM type DAC. Also shown in Fig. 15 are the outputs (B0 through B3) of binary counter 210 and outputs (L0 through L3) of 9-bit latch 211. For example, ANDing a counter output B1 with an inverted latch output L1 produces a pulse output X7 at the rising edge of a counter output B1. In this manner, pulse outputs (X8 through X0) are obtained. In the PDM type DAC, pulse select/synthesis circuit 203 selects pulse outputs X8 through X0 depending on the value of each of the bits of digital input data and then ORs them for the purpose of synthesis to generate a pulse string corresponding to the digital input data. For example, when digital input data is 320 (B101000000), reference pulses X8 and X6 are selected because their corresponding bits in the input data are 1, and then a pulse string is generated by synthesizing X8 and X6, and then sent to voltage conversion circuit 204 where its voltage is converted, and finally being input to integration circuit 205.

[0012] Fig. 16 is a diagram illustrating a relationship between each digital input data and its corresponding frequency of the pulse string for a PDM type DAC for liquid crystal displays. It is noted that the operating frequency (i.e., clock input) of a counter and latch is 120 MHz. As is seen from Fig. 16, as digital input data increases from 0 to 256, the frequency of the pulse string also increases monotonously, wherein it

reaches a maximum frequency of 60 MHz when the input data is 256, while as digital input data increases from 256 to 511, the frequency of the pulse string decreases monotonously. In this manner, since the frequency of the pulse string varies depending on digital input data (i.e., the number of switching times of a circuit for driving integration circuit 205 behind also varies), a degree of influence of switching upon the analog output voltage varies for each digital input data. This deteriorates the linearity of analog output voltage for DACs. Moreover, if the values of resistors and capacitors used for integration circuit 205 are set to match with pulse strings with low frequencies (i.e., around 0 or 511 of digital input data), the frequency of pulse strings becomes too high around a medium value (256) of the digital input data, resulting in unwanted power consumption.

## Summary of Invention

- [0013] In view of the technical problems described above, a feature of the present invention is to suppress adverse effects upon an analog output voltage due to switching depending on digital input data.
- [0014] Another feature of the invention is to suppress unwanted power consumption resulting from the number of switching times.
- [0015] According to the present invention, the number of switching times for pulse strings generated is configured to be smooth and constant without a local peak with respect to digital input data. Namely, the present invention provides a liquid crystal display that includes a liquid crystal cells forming an image display area on a substrate and a driver for applying a voltage to the liquid crystal cells based on a reference voltage for gamma correction corresponding to digital input data. The driver, which is mounted on the substrate and is comprised of a plurality of driver ICs connected via signal lines, keeps the number of switching times for pulse strings per time unit constant for a predetermined range of the digital input data when generating the pulse strings with pulse densities corresponding to the digital input data.
- [0016] Various other objects, features, and attendant advantages of the present invention will become more fully appreciated as the same becomes better understood when

considered in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the several views.

## Brief Description of Drawings

- [0017] Fig. 1 is a schematic diagram illustrating an embodiment of an image display unit the present invention is applied to.
- [0018] Fig. 2 depicts a schematic diagram of a PDM type of 9-bit DAC for generating gamma reference voltages according to the embodiment of the invention.
- [0019] Fig. 3 depicts details of a pulse generation circuit and pulse select/synthesis circuit according to the embodiment of the invention.
- [0020] Fig. 4 is a table illustrating a relationship between the number of divided bits and maximum frequencies of pulse strings when utilizing a pulse generation circuit and pulse select/synthesis circuits of the present invention.
- [0021] Fig. 5 depicts a schematic diagram of a pulse generation circuit in a PDM type DAC according to the present invention.
- [0022] Fig. 6 depicts a schematic diagram of a pulse generation circuit using method 1.
- [0023] Fig. 7 depicts reference pulse waveforms according to method 1 shown in Fig. 6.
- [0024] Fig. 8 is a diagram illustrating a relationship between digital input data and pulse string frequencies for a pulse generation circuit according to the present invention.
- [0025] Fig. 9 depicts a schematic diagram of a pulse generation circuit using method 3.
- [0026] Fig. 10 depicts reference pulse waveforms according to method 3 shown in Fig. 9.
- [0027] Figs. 11(a) and (b) depict a pulse generation circuit and pulse select/synthesis circuit, respectively, for a PDM type DAC based on 8 clock unit.
- [0028] Fig. 12 is a table comparing the size of pulse generation circuits between 4 clock unit and 8 clock unit.
- [0029] Fig. 13 depicts a configuration of a typical PDM type DAC.

[0030] Fig. 14 depicts a schematic diagram of a pulse generation circuit for use in a PDM type DAC for liquid crystal displays.

[0031] Fig. 15 depicts a waveform of pulse outputs (X8 through X5) of a PDM type DAC.

[0032] Fig. 16 is a diagram illustrating a relationship between each digital input data and its corresponding frequency of the pulse string for a PDM type DAC for liquid crystal displays.

## Detailed Description

[0033] The predetermined range of digital input data may be, for example, the digital input data ranging from 128 to 384 given a 9-bit digital-analog conversion circuit. Such a predetermined range may vary depending on the number of divided bits (W).

[0034] In another aspect of the invention, there is provided a driver for use in a liquid crystal display, that is characterized by having no local peak in the number of switching times for pulse strings per time unit when generating the pulse strings with pulse densities corresponding to the digital input data.

[0035] In a further aspect of the invention, there is provided a driver for use in a liquid crystal display, that is characterized by obtaining a reference voltage for gamma correction using pulse density modulation (PDM) as well as obtaining an output voltage using pulse width modulation (PWM) for a predetermined range of the digital input data around a medium value when generating pulse strings corresponding to the digital input data.

[0036] In a yet further aspect of the invention, there is provided a liquid crystal display driver such as a source driver for LCDs. In other words, the present invention provides a liquid crystal display driver for applying a voltage to liquid crystal cells forming an image display area, the driver includes a pulse generation circuit for generating a plurality of reference pulses in which pulse generation densities are weighted, a pulse select/synthesis circuit for generating a pulse string by selecting and synthesizing necessary reference pulses on the basis of digital input data and the reference pulses, and an integration circuit for integrating the pulse string generated by the pulse select/synthesis circuit to output a voltage (analog voltage) for gamma correction. The

number of switching times for the pulse string per time unit is unchanged for a predetermined range of the digital input data for gamma correction.

[0037] The pulse select/synthesis circuit outputs a logical sum between a carry output from an adder circuit, which has as its inputs high order  $W$  bits of the digital input data of  $n$  bits and low order  $W$  bits of a binary counter, and a logical product between outputs  $X(m-1)$  through  $X(0)$  of the pulse generation circuit where  $m=n-W$  and the digital input data  $D(m-1)$  through  $D(0)$ , thereby improving linearity for a wide range of input data such as when the number of divided bits is more than and equal to 3.

[0038] Furthermore, assuming that the digital input data is  $n$  bits and the number of divided bits is  $W$ , the pulse generation circuit outputs the reference pulses using an  $n$ -bit binary counter, an  $n-W$  bit latch, and  $n-W$  2-input gates. However, when  $W=2$ , an  $n-1$  bit latch and 2-input gates are required, while no adder (carry detection circuit) is needed.

[0039] In a still further aspect of the invention, there is provided a reference pulse generation circuit for generating reference pulses corresponding to  $n$ -bit digital input data includes a  $n$ -bit binary counter for counting up in synchronization with an input clock, a  $n-W$  bit latch for generating signals by delaying high order  $n-W$  bits output  $B(n-1)$  through  $B(W)$  from the binary counter by one input clock period, and  $n-W$  logical circuits for performing logical operations with receiving as inputs the high order  $n-W$  bits output  $B(n-1)$  through  $B(W)$  from the binary counter and the delayed signals corresponding to the high order  $n-W$  bits output  $B(n-1)$  through  $B(W)$  from the  $n-W$  bit latch and obtaining outputs  $X(0)$  through  $X(n-W-1)$  with lower reference pulse densities, whereas outputs  $X(n-W)$  through  $X(n-1)$  are obtained bypassing the logical circuits.

[0040] It is noted that when  $W=2$ ,  $n-1$  logical circuits are either  $n-1$  AND circuits or  $n-2$  AND circuits outputting  $X(0)$  through  $X(n-3)$  and a NOR circuit outputting  $X(n-2)$ .

[0041] In a further aspect of the invention, there is provided a reference pulse generation circuit for digital-analog conversion employing a pulse density modulation scheme includes means for generating reference pulses that are exclusively in a high state corresponding to digital input data, and means for generating the reference pulses

such that a number of switching times for pulse strings per time unit is constant for a predetermined range of the digital input data. It is noted that when  $W=2$ , the reference pulses are generated with the frequency thereof being kept constant for half the whole range of the digital input data. Generally speaking, the frequency is kept constant according to the ratio, that is,  $(2w-1-1)/2w-1$  with respect to the whole digital input data.

[0042] In another aspect of the invention, there is provided a method for generating reference pulses in a digital-analog converter includes the steps of generating pulse strings with pulse densities corresponding to digital input data that is input to the digital-analog converter, and keeping a number of switching times for the pulse strings per time unit constant for a predetermined range of the digital input data around a medium value. According to this, a maximum frequency of the pulse strings is reduced to less than half of that in the case where the number of switching times is not kept constant.

[0043] In a further aspect of the invention, there is provided a method for providing an analog voltage output used for a reference voltage for gamma correction in a source driver for a liquid crystal display includes the steps of for a range of the digital input data excluding a predetermined range around a medium value, integrating a pulse string, whose number of pulses is adjusted depending on the digital input data, to output an analog voltage; and for the predetermined range of the digital input data, integrating a pulse string, whose duty is adjusted depending on the digital input data, to output an analog voltage.

[0044] Now the present invention will be described with reference to the accompanying drawings illustrating preferred embodiments thereof.

[0045] Fig. 1 is a schematic diagram illustrating an embodiment of an image display unit the present invention is applied to. In the image display unit shown in Fig. 1, a liquid crystal module (LCD panel) is comprised of a liquid crystal cell control circuit 1 and liquid crystal cells 2 in a thin film transistor (TFT) structure. This liquid crystal module may be configured as a display unit separate from a host system such as a personal computer (PC) or as a display of a notebook PC. In liquid crystal cell control circuit 1, RGB video data (i.e., video signals) and control signals are input to an LCD controller 4



via a video interface (I/F) 3 from a graphics controller LSI (not shown) in the system. In general, DC power supply is also supplied through the video I/F 3.

[0046] DC-DC converter 5 generates a variety of DC power supply voltages necessary for liquid crystal cell control circuit 1 from DC power supply being supplied, and supplies them to a gate driver 6, a source driver 7 and a fluorescent tube for backlight (not shown), etc. LCD controller 4 processes signals received from video I/F 3 and supplies processed signals to gate driver 6 and source driver 7. Source driver 7 is responsible to supply a voltage to each of the source electrodes of TFTs arranged in a horizontal direction (X direction) in a TFT array, which is arranged in a matrix fashion on liquid crystal cells 2. Gate driver 6 is responsible to supply a voltage to each of the gate electrodes arranged in a vertical direction (Y direction) in a TFT array.

[0047] Both gate driver 6 and source driver 7 are comprised of multiple ICs. In the present embodiment, source driver 7 includes multiple source driver ICs 20 made of LSI chips. For convenience of explanation, liquid crystal cell control circuit 1 and liquid crystal cells 2 are shown to be divided in Fig. 1, however, multiple source driver ICs 20 are formed in the COG structure on a glass substrate where liquid crystal cells 2 are made, and furthermore each wiring is also made on the glass substrate in the WOA structure, according to the embodiment of the present invention.

[0048] In this manner, particularly for LCDs for a frame with narrow rims around a display area, the cost of LCD panel is reduced by mounting source driver 7 directly on the TFT glass substrate of the LCD panel and implementing wiring between source drivers ICs 20 using aluminum wiring on the glass substrate. Since a sufficient wiring area could not be reserved for such LCD panels, there may be a case where a reference voltage for gamma correction, which would be typically generated on an LCD panel board (PCB), is produced in individual source driver ICs 20. In this case, a high-precision digital-analog conversion circuit (DAC) is required in order to equalize the reference voltages for gamma correction produced in each of the source driver ICs 20. Since dispersion of resistors and capacitors created on the chip is great, the current summing scheme such as an R-2R ladder network type DAC is considered to be inappropriate. Thus, the present embodiment uses a PDM type DAC relying on the time control scheme.

[0049] Fig. 2 depicts a schematic diagram of a PDM type of 9-bit DAC for generating gamma reference voltages according to the embodiment of the invention. According to the embodiment, a gamma reference voltage generation circuit as shown in Fig. 2 is provided for each of the source driver ICs 20 in source driver 7 of LCD. The circuit shown in Fig. 2 comprises a pulse generation circuit 21 for generating a plurality of reference pulses in which pulse generation densities are weighted, digital input data latches 22 for storing digital input data serving as gamma correction data, pulse select/synthesis circuits 23 for generating a pulse string by selecting and synthesizing necessary reference pulses on the basis of generated reference pulses and stored input data, voltage conversion circuits 24 for converting a pulse string generated by a digital power supply into a desired analog voltage range, and integration circuits (low pass filters) 25 for converting a pulse string into an analog voltage. Pulse generation circuit 21 is the most characteristic component in the embodiment, while digital input data latches 22 through integration circuits (low pass filters) 25 are provided as many as necessary gamma correction reference voltages, respectively.

[0050] In the embodiment, there is provided a DAC with a frequency characteristic having a trapezoidal shape, for example, in contrast to a triangular shape shown in Fig. 16 with a peak at 256, whereby the operating frequency is reduced compared with a conventional relationship between digital input data and a pulse string frequency shown in Fig. 16. Accordingly, a DAC of the present invention employs a pulse density modulation (PDM) scheme in a range of the digital input data other than a predetermined range around a medium value, while employing a pulse width modulation (PWM) scheme in the predetermined range around a medium value in order to avoid the increase of frequencies.

[0051] Fig. 3 depicts details of pulse generation circuit 21 and pulse select/synthesis circuit 23. Here is shown how to generate pulses for an n-bit DAC assuming the digital input data is n bits rather than 9 bits. A synthesized pulse output obtained by the circuit shown in Fig. 3 is represented as a logical sum between a carry output from an adder circuit that receives as its inputs high order W bits of gamma data and low order W bits of binary counter outputs, and a logical product between outputs  $X(m-1)$  through  $X(0)$  of pulse generation circuit 21 and gamma data  $D(m-1)$  through  $D(0)$ . Note that in the case of n-bit DAC,  $n-1 \geq m \geq 0$ ,  $k=n-1-m$ ,  $w=n-m$ .

[0052] Fig. 4 is a table illustrating a relationship between the number of divided bits and a maximum frequency of a pulse string when utilizing pulse generation circuit 21 and pulse select/synthesis circuits 23 of the present invention. It is seen that the maximum frequency of the generated pulse string varies depending on a value of the number of divided bits ( $W$ ) so that the region also varies where the frequency of the pulse string is kept constant. It is also seen that as a value of  $W$  increases, the frequency of a pulse string decreases, however, the scale of the adder circuit will inconveniently increase.

[0053] As shown in Fig. 4, when  $W=1$ , the adder circuit is composed of only 2-input AND gates, thus resulting in a conventional PDM type DAC. When  $W=2$ , this is a special case where the circuit is simplified most because carry detection can be implemented by using only 2-input AND gates without using an adder circuit. In this case, the maximum frequency of the pulse string is  $f/2$  (Hz) and a ratio of a region, where the number of switching times is constant, to the whole input data is  $1/2$ . When  $W$  is more than or equal to 3, the frequency decreases compared with when  $W=2$ , the adder circuit is required to detect a carry, so that the scale of the circuit increases. In addition, the scale of integration circuit 25 following the synthesis circuit also increases. When  $W=n$ , the circuit becomes the same configuration as a PWM type DAC.

[0054] Fig. 5 depicts a schematic diagram of pulse generation circuit 21 in a PDM type DAC according to the present invention. This pulse generation circuit 21 comprises  $n$ -bit binary counter 31,  $n-1$  bit latch 32, and  $n-1$  2-input AND gates 33. As an output of pulse generation circuit 21, there is provided a logical product by 2-input AND gates 33 between outputs of  $n$ -bit binary counter 31 and outputs of  $n-1$  bit latch 32. Namely,  $n-1$  bit latch 32 generates a signal by delaying high order  $n-1$  bits output  $B(n-1)$  through  $B(1)$  from  $n$ -bit binary counter 31 by one input clock period, and then 2-input AND gates 33 perform a logical operation with receiving as inputs the high order  $n-1$  bits output  $B(n-1)$  through  $B(1)$  from  $n$ -bit binary counter 31 and delayed signals corresponding to the high order  $n-1$  bits output  $B(n-1)$  through  $B(1)$  from  $n-1$  bit latch 32.

[0055] It is preferable that the pulse generation circuit for liquid crystal display DACs generates pulses using a method in which the number of switching times does not

vary in the midsection of the digital input data, in consideration of linearity after the pulse generation. Here is now described a method for improving linearity by taking a case by way of example where a pulse string is considered in units of 4 clock when the number of divided bits  $W=2$ . Based on a 4 clock unit, there exist four methods for embedding pulses corresponding to higher bits in order to increase the pulse density in the block along with the increase of the digital input data. Below is shown how the number of bits increases according to these four methods:

[0056] Method 1: 0000 → P000 → 0001 → P001 → 0110 → P110 → 0111 → P111 → 1111

[0057] Method 2: 0000 → P000 → 0001 → P001 → 0011 → P011 → 0111 → P111 → 1111

[0058] Method 3: 0000 → P000 → 0100 → P100 → 0110 → P110 → 0111 → P111 → 1111

[0059] Method 4: 0000 → P000 → 0100 → P100 → 0011 → P011 → 0111 → P111 → 1111

[0060] It is noted that P is a pulse depending on modulation data. Now a reference pulse generation circuit of the present invention will be described below that uses the above methods 1 and 3 to reduce the scale of the circuits.

[0061] Fig. 6 depicts a schematic diagram of pulse generation circuit 21 using the above method 1. There is shown a 9-bit DAC that comprises 9-bit binary counter 41, 8-bit latch 42, and eight 2-input AND gates 43. 9-bit binary counter 41 counts up in synchronization with an input clock and supplies counter outputs B8 through B1. Corresponding to those counter outputs B8 through B1, there are generated latch outputs L8 through L1 that are the signals delayed by one input clock period with 8-bit latch 42. These signals are processed according to the logical expression shown in the above method 1 to generate reference pulse outputs X8 through X0. Considering a general case shown in Fig. 5, when  $n=9$ , 2-input AND gates 43 perform a logical operation with receiving as inputs the high order  $n-1$  bits output B(8) through B(1) and delayed signals corresponding to those high order  $n-1$  bits output from 8-bit latch 42 and then output X(0) through X( $n-2$ ). Note that output X( $n-1$ ), that is, X8 is output without passing through the logical circuit, as shown in Fig. 6.

[0062] The logical expression for the pulse generation circuit shown in Fig. 6 (i.e., Method 1) are summarized as follows:

- [0063]      $X8 \leq \text{not } L1$ ; Logical expression (1)
- [0064]      $X7 \leq B1 \text{ and } L1$ ; Logical expression (2)
- [0065]      $X6 \leq B2 \text{ and (not } L2)$ ; Logical expression (3)
- [0066]      $X5 \leq B3 \text{ and (not } L3)$ ; Logical expression (4)
- [0067]      $X4 \leq B4 \text{ and (not } L4)$ ; Logical expression (5)
- [0068]      $X3 \leq B5 \text{ and (not } L5)$ ; Logical expression (6)
- [0069]      $X2 \leq B6 \text{ and (not } L6)$ ; Logical expression (7)
- [0070]      $X1 \leq B7 \text{ and (not } L7)$ ; Logical expression (8)
- [0071]      $X0 \leq B8 \text{ and (not } L8)$ ; Logical expression (9)

[0072]     The above logical expression (1) reduces the frequency of the reference pulse output X8 to half, while the above logical expression (2) shifts the pulse generation position of the reference pulse output X7 by 1 clock. Assuming that the density of reference pulse X0 is 1, the densities of reference pulses X1, X2, X3, X4, X5, X6, X7 and X8 generated by this scheme are 2, 4, 8, 16, 32, 64, 128 and 256, respectively. Since the reference pulses X0 through X8 are generated such that they become high exclusively, these pulses never overlap temporally each other even if any plural number of reference pulses are synthesized.

[0073]     Fig. 7 depicts reference pulse waveforms according to method 1 shown in Fig. 6. As is seen from the drawing, the pulses X6 through X0 are generated such that they become high in the timing next to when X8 and X7 are in a high state. Accordingly, as the digital input data increases within a range of 0 to 128, the frequency of the pulse string increases monotonously, whereas X8 or X7 is selected for the digital input data within a range of 128 to 384, wherein any of X6 through X0 in the high state selected at the same time is combined to the high state of X8 or X7. Therefore, the frequency of the synthesized pulse string is kept constant for the digital input data ranging from 128 to 384. For the digital input data ranging from 384 to 511, as the input data increases, the frequency of the pulse string decreases monotonously. The above also applies to an n-bit DAC other than 9-bit DAC.

[0074] Fig. 8 is a diagram illustrating a relationship between digital input data and its corresponding frequency of the pulse string for pulse generation circuit 21 according to the invention, wherein the input clock is 120 MHz. As is seen by comparing with the prior art shown in Fig. 16, the frequency of the pulse string is kept constant for the digital input data within a range of 128 to 384. In this way, using pulse generation circuit 21 of the present invention, the maximum frequency of the pulse string is able to be reduced to half. When generating an analog output voltage in this range, the number of switching times for voltage conversion circuits 24 to drive integration circuit 25 is able to be kept constant. Accordingly, the adverse effect on the analog output voltage due to switching is maintained uniformly, thus the linearity is expected to be improved. When driving the liquid crystal display at 5 V, this range, that is, 128 to 384 of digital input data corresponds to 1.25V to 3.75V of analog output voltage whose dynamic range is between 0V and 5V. This range corresponds to a portion where the liquid crystal display changes most steeply, and which is most sensitive, that is, the most important voltage range to drive the liquid crystal display. Therefore, it is clear that a great effect is brought about by the present invention.

[0075] Fig. 9 depicts a schematic diagram of pulse generation circuit 21 with  $W=2$  using the above method 3 apart from that shown in Fig. 6. As with the case in Fig. 6, there is shown a 9-bit DAC that comprises 9-bit binary counter 51, 8-bit latch 52, and eight 2-input AND gates 53. Unlike the method 1 shown in Fig. 6, one NOR circuit is provided instead of an AND circuit. As with Fig. 6, 9-bit binary counter 51 counts up in synchronization with an input clock and supplies counter outputs B8 through B1. Corresponding to those counter outputs B8 through B1, there are generated latch outputs L8 through L1 that are the signals delayed by one input clock period with 8-bit latch 52. These signals are processed according to the logical expression shown in the above method 3 to generate reference pulse outputs X8 through X0.

[0076] The logical expression for the pulse generation circuit shown in Fig. 9 (i.e., Method 3) are summarized as follows:

[0077]  $X8 \leq B1$ ; Logical expression (1')

[0078]  $X7 \leq B1 \text{ nor } L1$ ; Logical expression (2')

[0079]  $X6 \leq B2$  and (not L2); Logical expression (3)

[0080]  $X5 \leq B3$  and (not L3); Logical expression (4)

[0081]  $X4 \leq B4$  and (not L4); Logical expression (5)

[0082]  $X3 \leq B5$  and (not L5); Logical expression (6)

[0083]  $X2 \leq B6$  and (not L6); Logical expression (7)

[0084]  $X1 \leq B7$  and (not L7); Logical expression (8)

[0085]  $X0 \leq B8$  and (not L8); Logical expression (9)

[0086] The above expressions (1') and (2') are different from those of method 1 shown in Fig. 6, while the others are the same as in method 1. The above logical expression (1') reduces the frequency of the reference pulse output X8 to half, while the logical expression (2) shifts the pulse generation position of the reference pulse output X7 by 1 clock. Assuming that the density of reference pulse X0 is 1, the densities of reference pulses X1, X2, X3, X4, X5, X6, X7 and X8 are 2, 4, 8, 16, 32, 64, 128 and 256, respectively. Since the reference pulses X0 through X8 are generated such that they become high exclusively, these pulses never overlap temporally each other even if any plural number of reference pulses are synthesized.

[0087] Fig. 10 depicts reference pulse waveforms according to method 3 shown in Fig. 9. As with Fig. 7, the pulses X6 through X0 are generated such that they become high in the timing next to when X8 and X7 are in a high state. Accordingly, as the digital input data increases within a range of 0 to 128, the frequency of the pulse string increases monotonously, whereas X8 or X7 is selected for the digital input data within a range of 128 to 384, wherein any of X6 through X0 in the high state selected at the same time is combined to the high state of X8 or X7. Therefore, the frequency of the synthesized pulse string is kept constant for the digital input data ranging from 128 to 384. For the digital input data ranging from 384 to 511, as the input data increases, the frequency of the pulse string decreases monotonously. It is noted that the relationship between digital input data and a pulse string frequency when using the above method 3 shown in Figs. 9 and 10 is the same as that shown in Fig. 8, thereby achieving the same effects.

[0088] Next, let's consider the case where the number of divided bits  $W=3$ , that is, a pulse string is considered on an 8 clock basis. Here is now described a method where the pulse density in blocks increases along with the increase of digital input data. Based on an 8 clock unit, there exist two methods for increasing the pulse density in the block along with the increase of the digital input data. Below is shown how the number of bits increases according to these two methods:

[0089] Method 1: 00000000 → P0000000 → 00000001 → P0000001 → 00000011 → P0000011 → 00000111 → P00000111 → 00001111 → P0001111 → 00011111 → P0011111 → 00111111 → P0111111 → 01111111 → P1111111 → 11111111

[0090] Method 2: 00000000 → P0000000 → 01000000 → P1000000 → 01100000 → P1100000 → 01110000 → P1110000 → 01111000 → P1111000 → 01111100 → P1111100 → 01111110 → P1111110 → 01111111 → P1111111 → 11111111

[0091] It is noted that P is a pulse depending on modulation data.

[0092] Since the scale of the reference pulse generation circuit using the above method 2 becomes large, here is now be described about the reference pulse generation circuit using the above method 1.

[0093] Figs. 11(a) and (b) depict pulse generation circuit 21 and pulse select/synthesis circuit 23 for a PDM type DAC based on 8 clock unit, wherein Fig. 11(a) shows pulse generation circuit 21 and Fig. 11(b) shows pulse select/synthesis circuits 23. Pulse generation circuit 21 shown in Fig. 11(a) comprises 9-bit binary counter 61, 6-bit latch 62, and six 2-input AND gates 63. On the other hand, pulse select/synthesis circuits 23 shown in Fig. 11(b) comprises a synthesis circuit 65 including 2-input AND gates and 3-input OR gates, and an adder circuit 66 serving as a carry detection section.

[0094] In order to generate pulse modulation with 8 clocks, outputs B0, B1 and B2 of binary counter 61 are directly input to adder circuit 66 shown in Fig. 11(b) without being latched. The frequency of the synthesized pulse string is kept constant for the digital input data within the range of 64 to 448. Compared with the case of 4 clock unit, the pulse string frequency is further reduced to half while the number of gates increases.



[0095] Fig. 12 is a table comparing the size of pulse generation circuit 21 between 4 clock unit and 8 clock unit. The former is based on pulse generation circuit 21 shown in Fig. 6, while the latter is based on pulse generation circuit 21 shown in Fig. 11(a). As seen from Fig. 12, considering the pulse synthesis section for 10 sets, the number of gates required for the 8 clock unit is 1.4 times that of the 4 clock unit. Therefore, the 4 clock unit is superior in terms of the circuit scale, while the 8 clock unit is superior in terms of the frequency.

[0096] As described above, according to the embodiment of the invention, the frequency is reduced for a predetermined range of digital input data around its medium value to keep the number of switching times constant, thereby reducing the power consumption of a PDM type DAC for the liquid crystal display and improving linearity of output voltage. As a result, linearity of analog output voltage is improved, which allows to reduce deviation of reference voltages for gamma correction between each of the source driver ICs 20. Furthermore, compared with typical PDM type DACs, wasted power consumption is reduced, thereby reducing power consumption of LCD panels advantageously.

[0097] When the number of divided bits  $W=2$  as shown in Fig. 6 through Fig. 10, an effect is brought out for digital input data within a range of 128 to 384 at 9-bit DAC. As described above, this corresponds to 1.25V to 3.75V of analog output voltage when driving the liquid crystal display at 5 V and which is the most important voltage range, thus the great effect is expected according to the present invention. When it is necessary to improve linearity in an even wider range and to reduce the operating frequency, pulse generation circuit 21 and pulse select/synthesis circuits 23 shown in Fig. 11(a) and (B) may be used. Namely, considering the trade-off between the improvement of linearity and the circuit scale based on the characteristics shown in Fig. 4 to determine an appropriate number of divided bits for pulse generation circuit 21, an optimal configuration for a target LCD can be obtained.

[0098] The present invention has been described with respect to DACs implementing a reference voltage generation circuit for gamma correction in a liquid crystal display, however, the invention is also applicable to reference pulse generation circuits in other fields, including a DAC used for measuring instruments. However, by applying

the present invention to an LCD implementing WOA, a great improvement will be achieved in terms of both linearity and the circuit scale reduction.

[0099] As mentioned above, according to the present invention, it becomes possible to suppress adverse effects upon an analog output voltage due to switching depending on digital input data.

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